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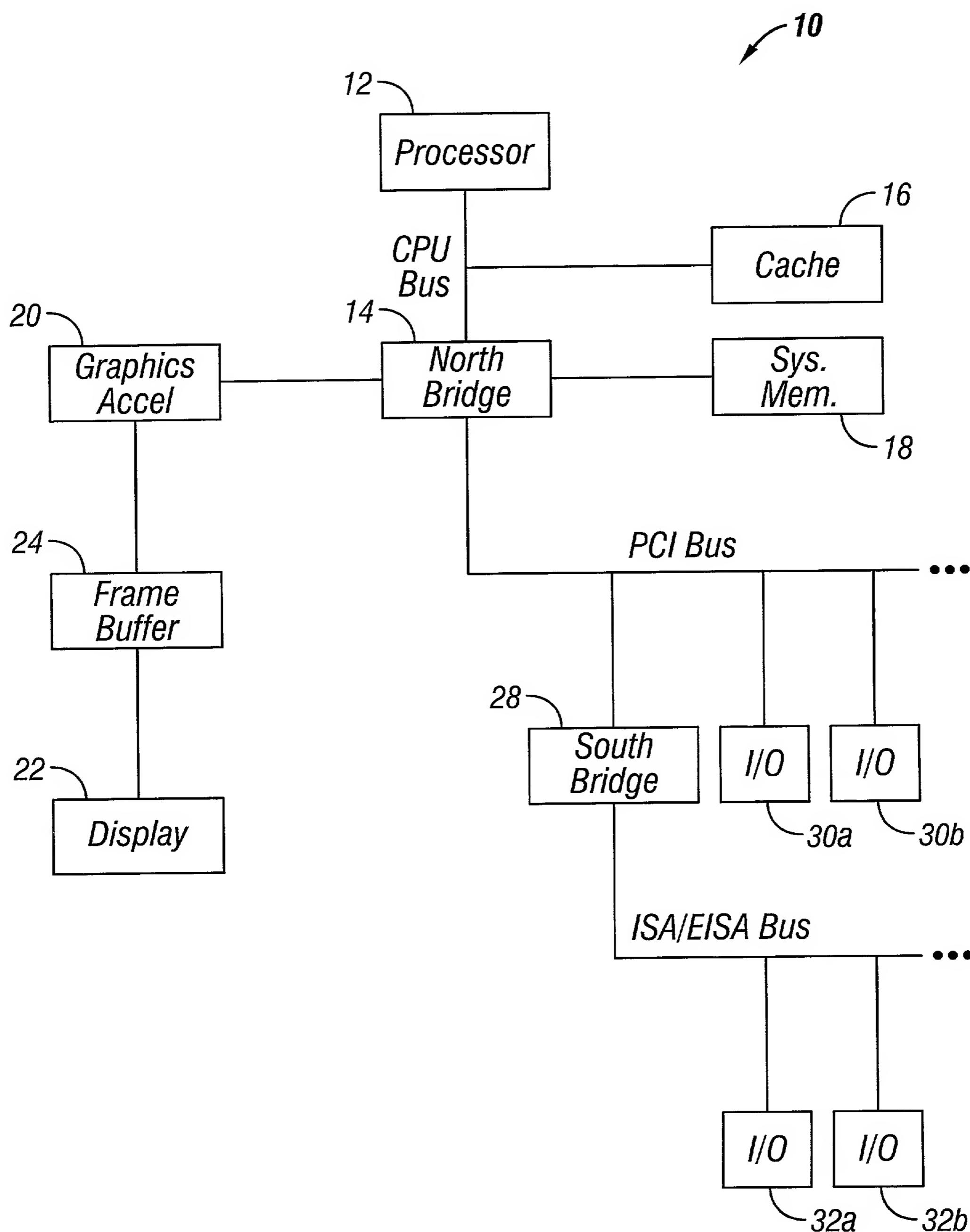


FIG. 1

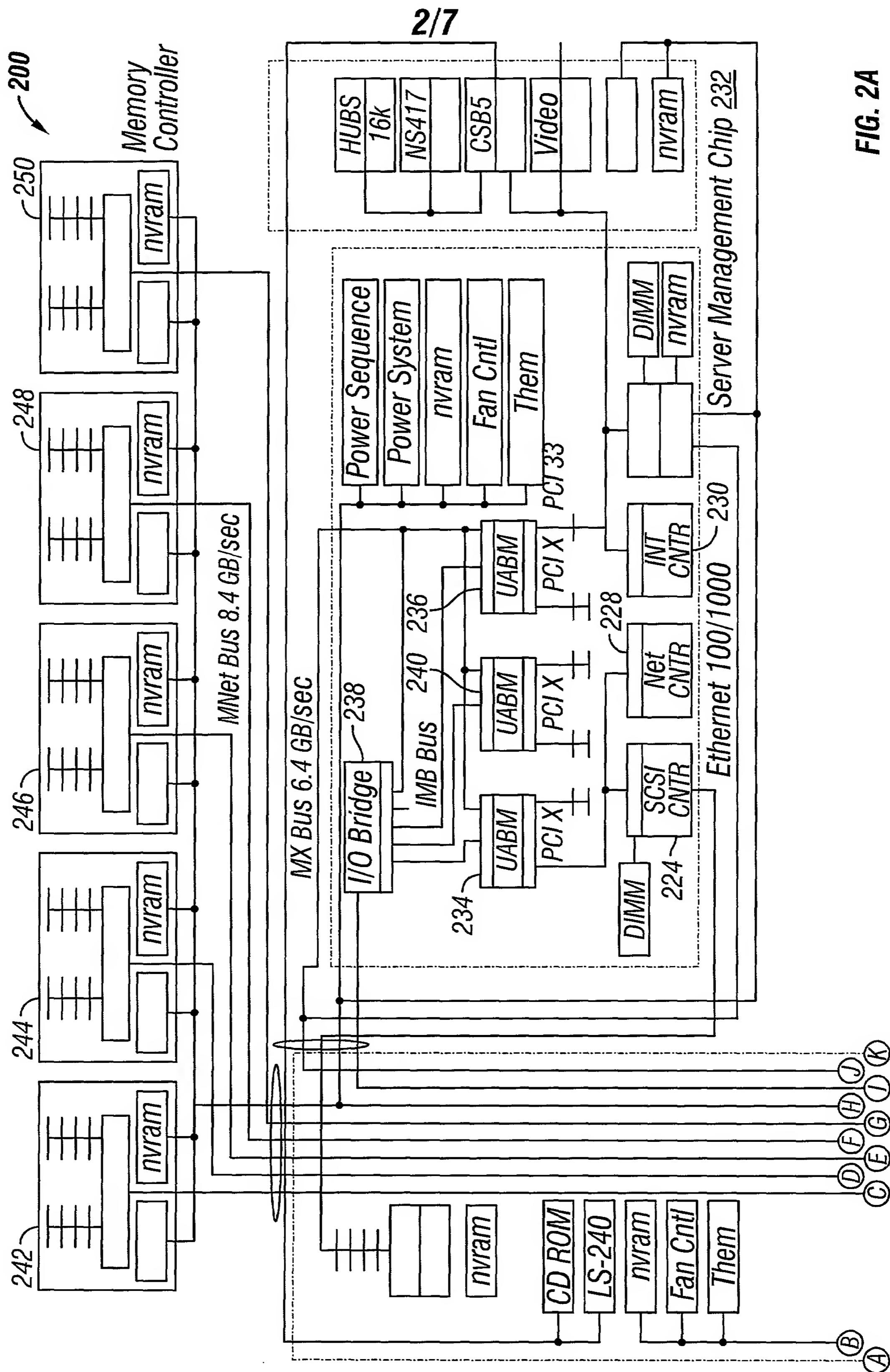


FIG. 2A

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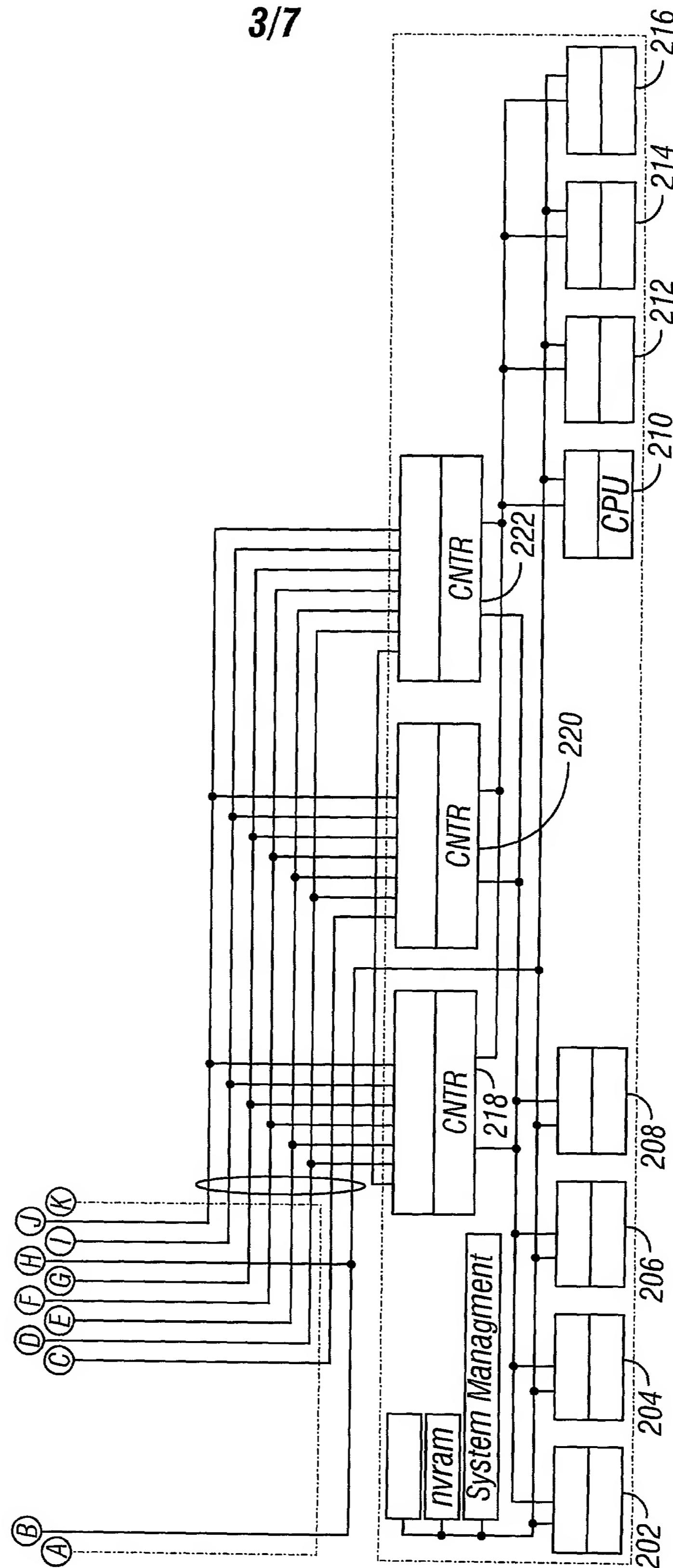
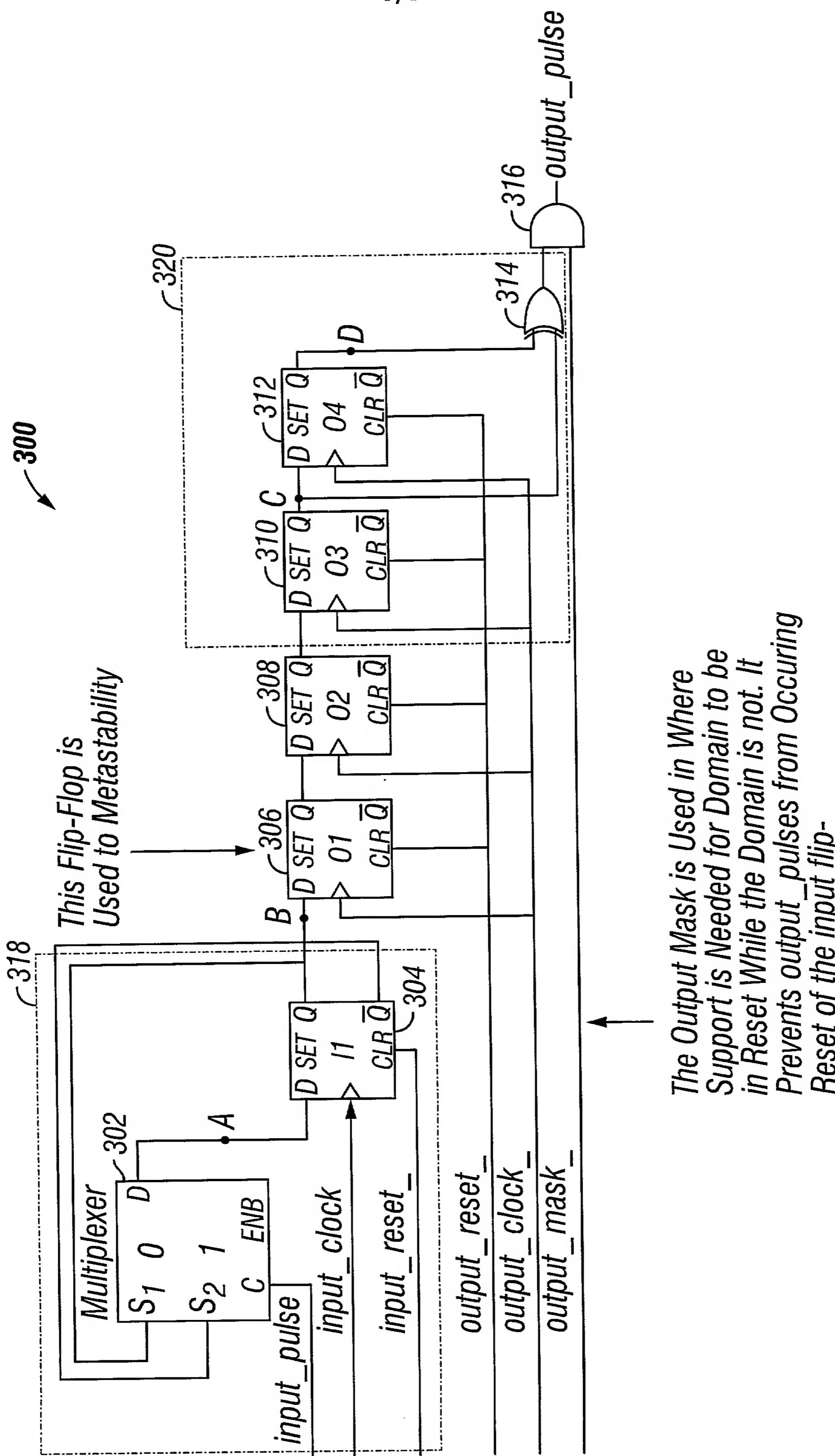


FIG. 2B



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*Universal Asynchronous Boundary Module - Case:
Input Clock Domain Reset Asserted*

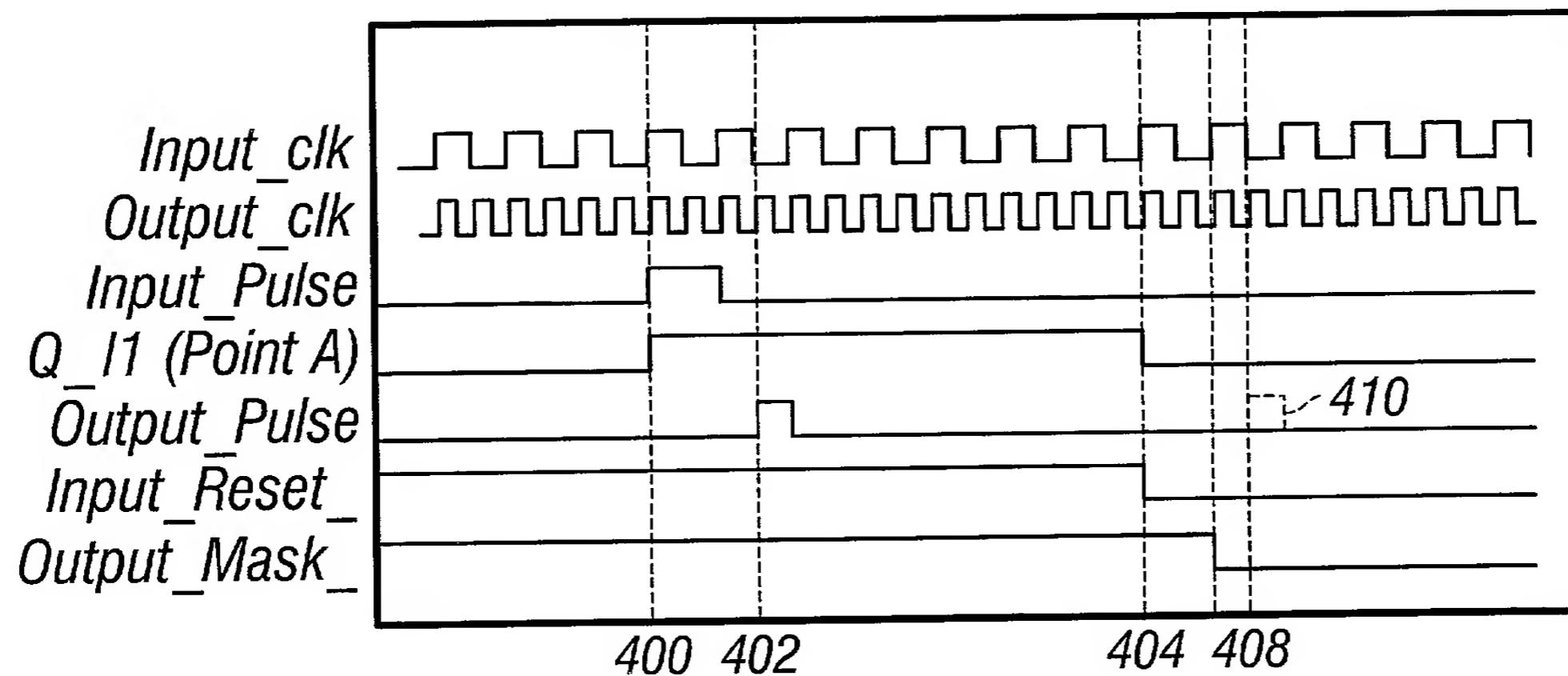


FIG. 4

*Universal Asynchronous Boundary Module - Case:
Output Clock Domain Reset Asserted*

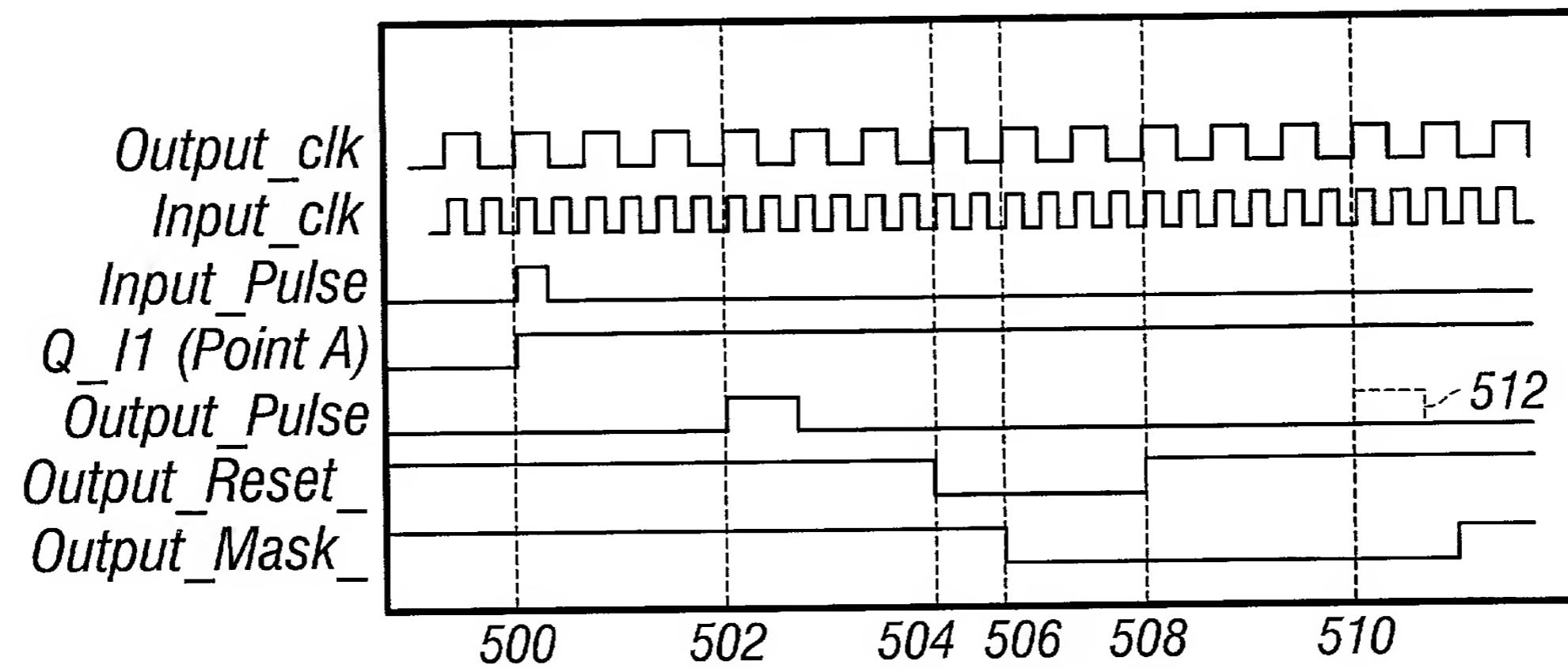


FIG. 5

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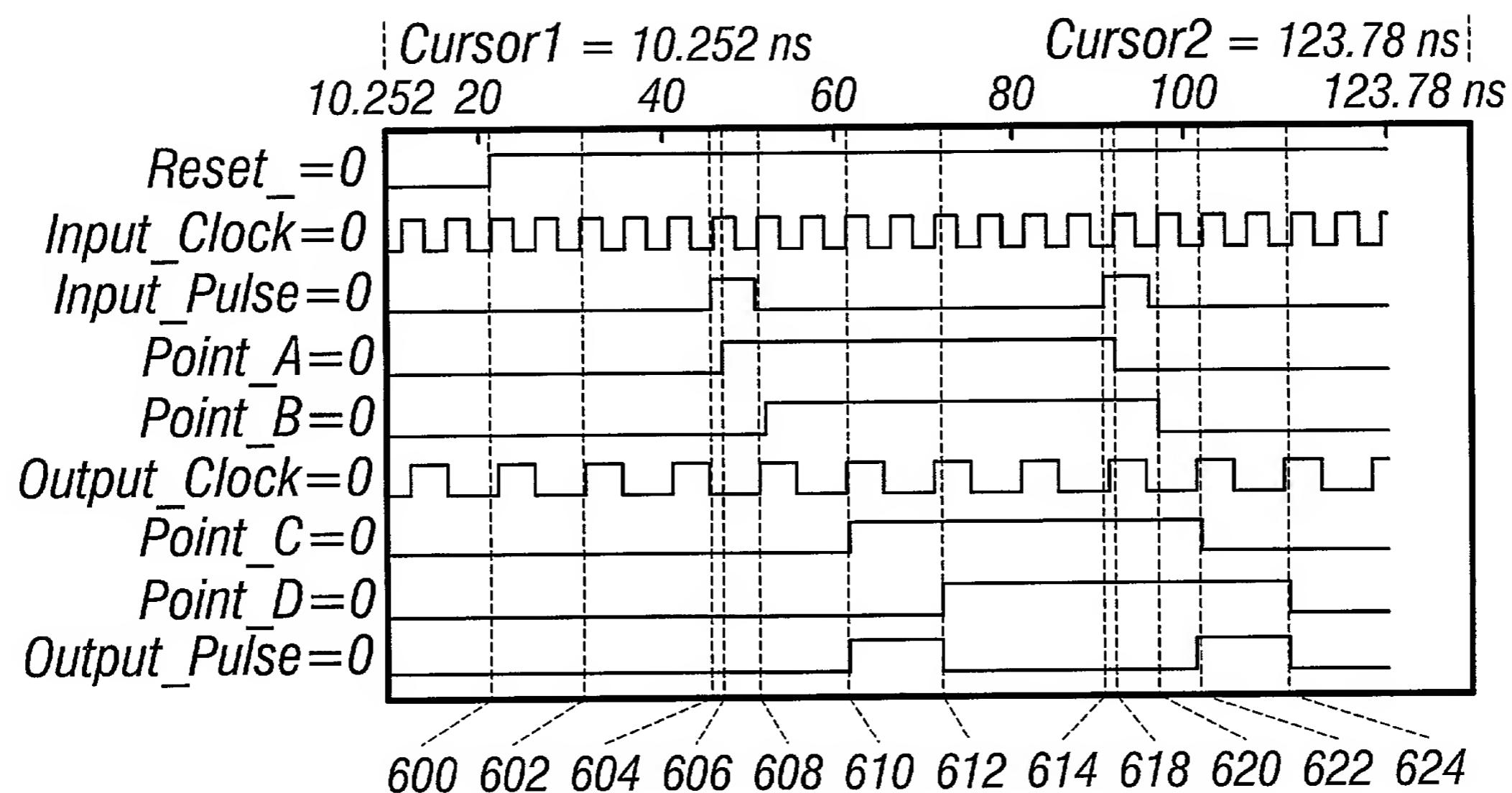


FIG. 6

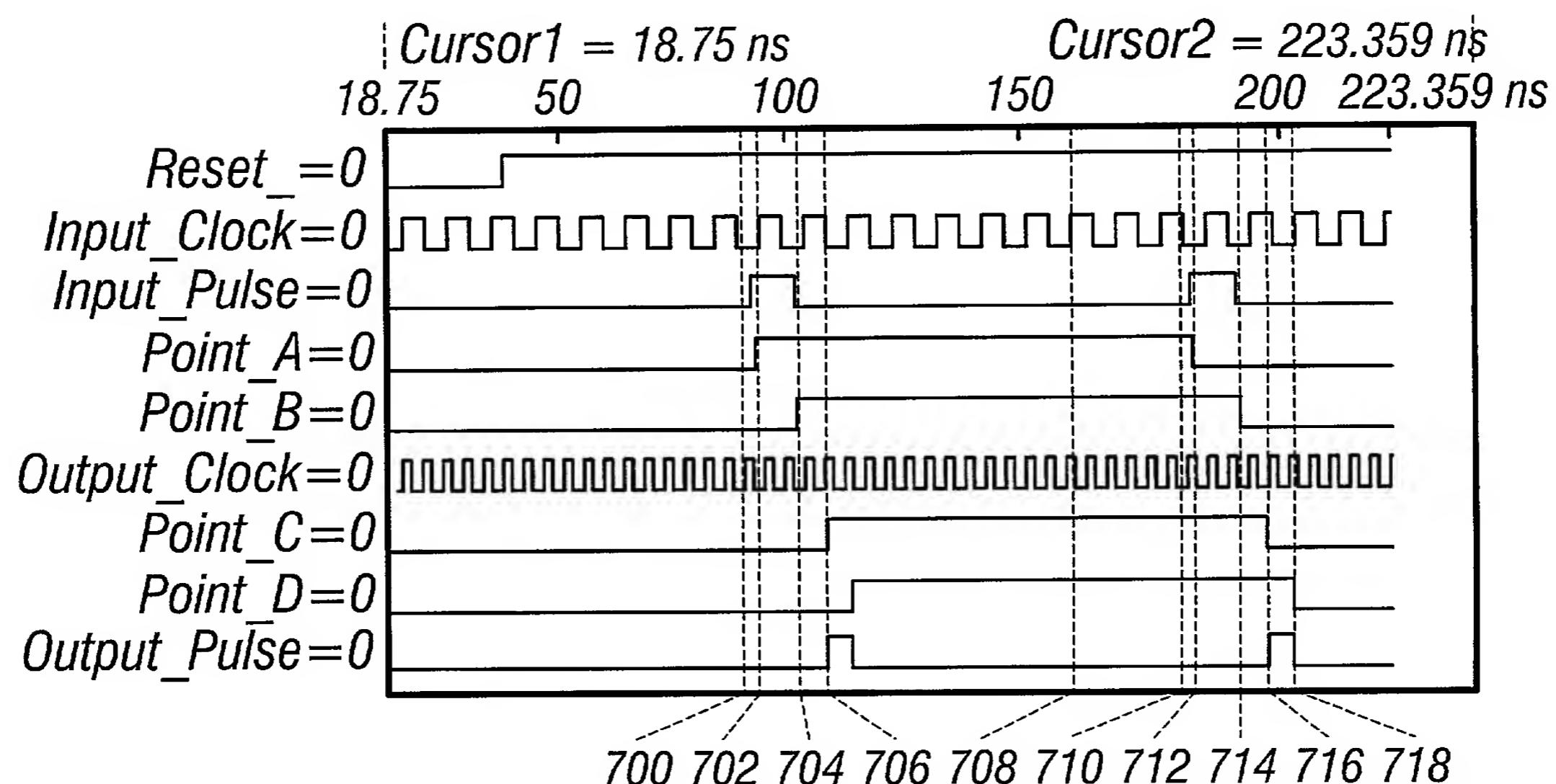


FIG. 7

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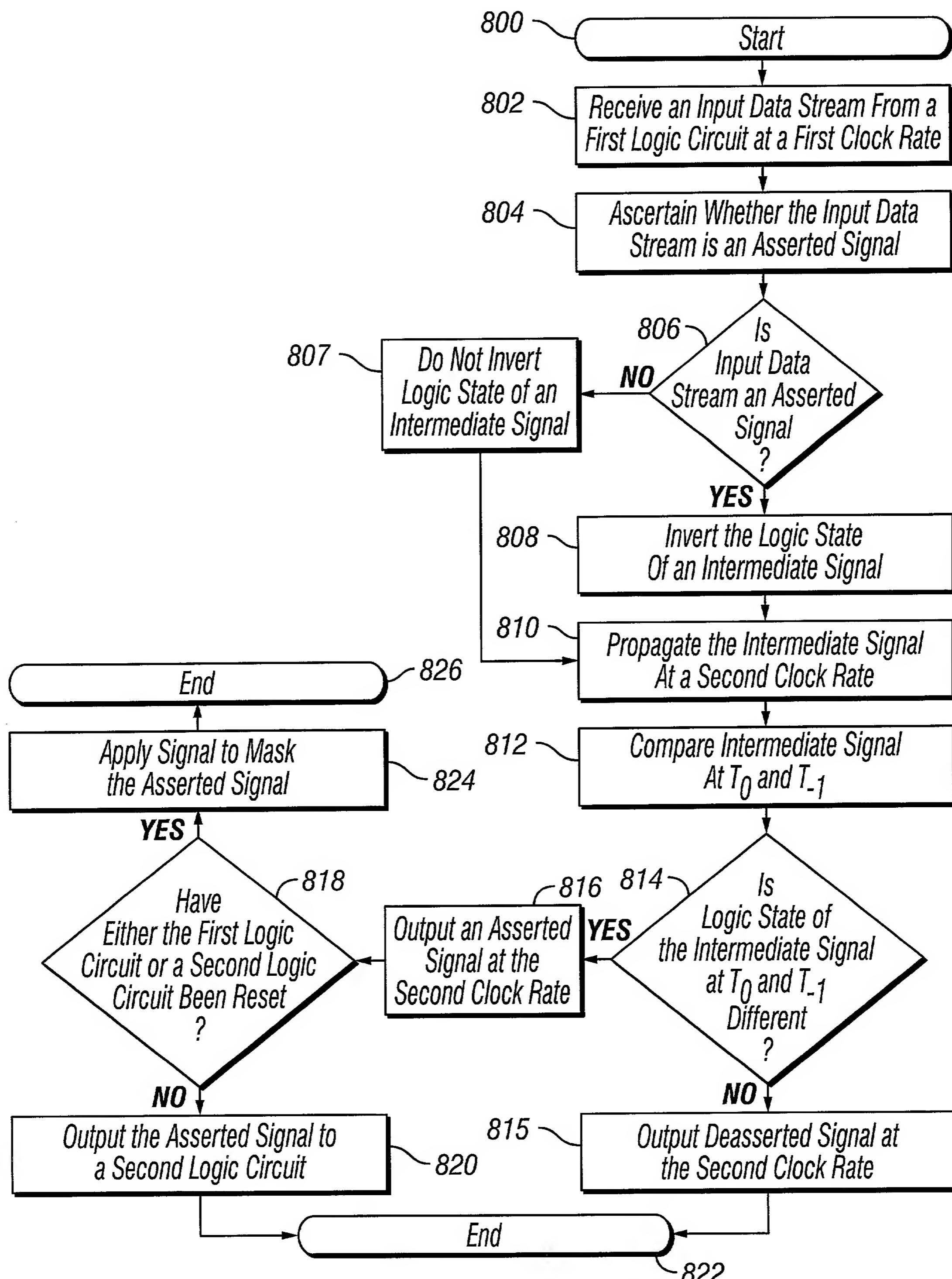


FIG. 8